

# Design of a High-Speed Reference Selector Switch Module for the Coherent Reference Generator Assembly

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*Design effort was started in April 1973 to develop and fabricate a high-speed switch module for the Coherent Reference Generator Assembly. The major design goal was to develop a high-speed switch capable of switching between frequency standards in less than 400 ns in the event of a primary standard failure, thus providing a constant failsafe 1-MHz reference signal to the station clocks. This report reviews the overall design and provides a general overview of the completed module.*

The engineering model of the Coherent Reference Generator Assembly (CRG) was installed and implemented at DSS 14 during July 1973. Included in this installation was an engineering prototype of the 1-MHz clock reference switch module (switch module), which supplies 1-MHz reference signals to the frequency and timing subsystem (FTS) clock and timing circuits.

The following significant features of the Switch Module will be discussed in this report:

- (1) Design objective.
- (2) System application.
- (3) Description.
- (4) Present status.

## I. Design Objective

The major design objective for the switch module was to provide a constant 1-MHz reference to the station clock by automatically switching to a backup reference source in less than 400 ns in the event of a primary source failure.

## II. System Application (Fig. 1)

Inputs to the CRG are obtained directly from the station frequency standards that, during the next few years, may be two rubidium standards (Rb) or two hydrogen maser (HM) standards.

The primary input to the FTS clock system from the CRG is a failsafe 1-MHz reference derived from either

the present rubidium standards or the future ultrastable hydrogen maser standards. Once a class of standard is chosen (either rubidium or hydrogen maser), the secondary or backup reference is derived from the same generic type (i.e., if hydrogen maser No. 2 is chosen as the prime standard, hydrogen maser No. 1 would be the backup unit).

Both the primary and secondary standard 1-MHz references are made available to the FTS so that duplicate clocks can be operated for long-term stability and standard performance determination.

### III. Description (Fig. 2)

The switch module is housed in a standard Block IV RF module and has been designed to operate without operator adjustment or alignment.

The switch module has been designed with a "failsafe" dc power system. In the event of a dc power loss from the CRG power supplies, the module automatically switches to a battery backup source located in the FTS, thus assuring continuous 1-MHz references to the station clock.

Two input references are selected, within the module, by a solid-state multiplexer that is addressed externally by the CRG control and monitor panel. The multiplexer's logic assures that the primary signal is obtained from the selected frequency standard and the secondary, or backup, is derived from the other like standard.

The key idea of the overall switch design is to use digital switching techniques to accomplish the high-speed switching. To accomplish this, both the primary and secondary standard inputs are passed through Schmitt triggers and converted to transistor-transistor logic (TTL) levels.

To detect primary standard failure, two parameters must be considered: (1) instantaneous signal presence, and (2) the average input power level.

Instantaneous failure sensing and switching is accomplished through an unusual application of a zero cross-over detector circuit, which consists of two voltage comparator integrated circuits interconnected and biased to provide full 360-deg signal presence sensing of the primary input signal.

If the input signal is present, the failure sensor remains at a logical "1" level. If the input signal should disappear

for a time interval in excess of approximately 250 ns, the sensor output assumes a logical "0" level thus initiating a failure mode signal. The 250-ns decision time is established by a simple resistor-capacitor (RC) filter in the sensor output, which prevents switch operation on minor noise disturbances.

The failure mode signal triggers a one-shot retriggerable multivibrator circuit initiating the switching gate that gates off the primary signal channel and enables the secondary in its place. The transfer from primary to secondary signal, after primary failure, is accomplished in less than 400 ns.

The one-shot multivibrator serves an essential function by assuring that once a failure has been sensed and a transfer between standards effected, approximately a one-half second delay is required before the circuit can revert back to normal operation. This prevents the switch from chattering on an intermittent input signal.

Average power sensing and switching are accomplished by measuring the primary input power with a signal level detector. If the input power remains above a preset level of approximately +9 dBm, the primary level sense signal remains at a logical "1." If, however, the input level falls below this preset level, the primary level sense signal assumes a logical "0" state initiating a switching gate to disable the primary channel and enable the secondary in its place.

Level monitor logic is also designed to provide continuous module status information to the CRG control and monitor panel. Input and output signal power levels are monitored in individual level detector circuits and are compared in an exclusive "or" circuit. If inputs are above the preset level of approximately +9 dBm, output from the module must also be present and above +9 dBm, or the module "output failure" signal will be initiated. If no inputs are present or they fall below the +9-dBm level, outputs are not expected and only the "input failure" signals will be initiated.

The TTL signals are filtered at the switch output to provide sine wave outputs, at nominal 50-ohm impedance, so that no changes to the existing FTS are required.

### IV. Status

Documentation is complete and the first production model of the switch module has been built and tested. Installation at DSS 14 will be accomplished as soon as the station operational freeze is lifted.

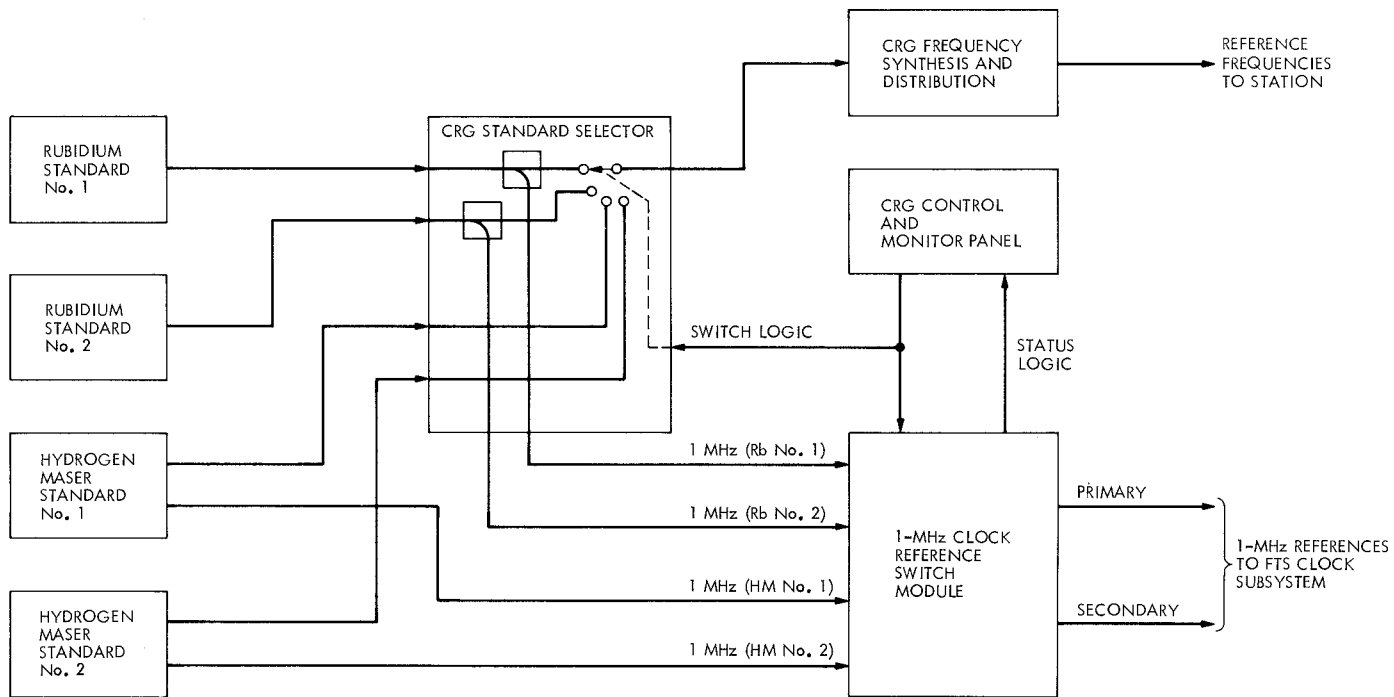


Fig. 1. System block diagram

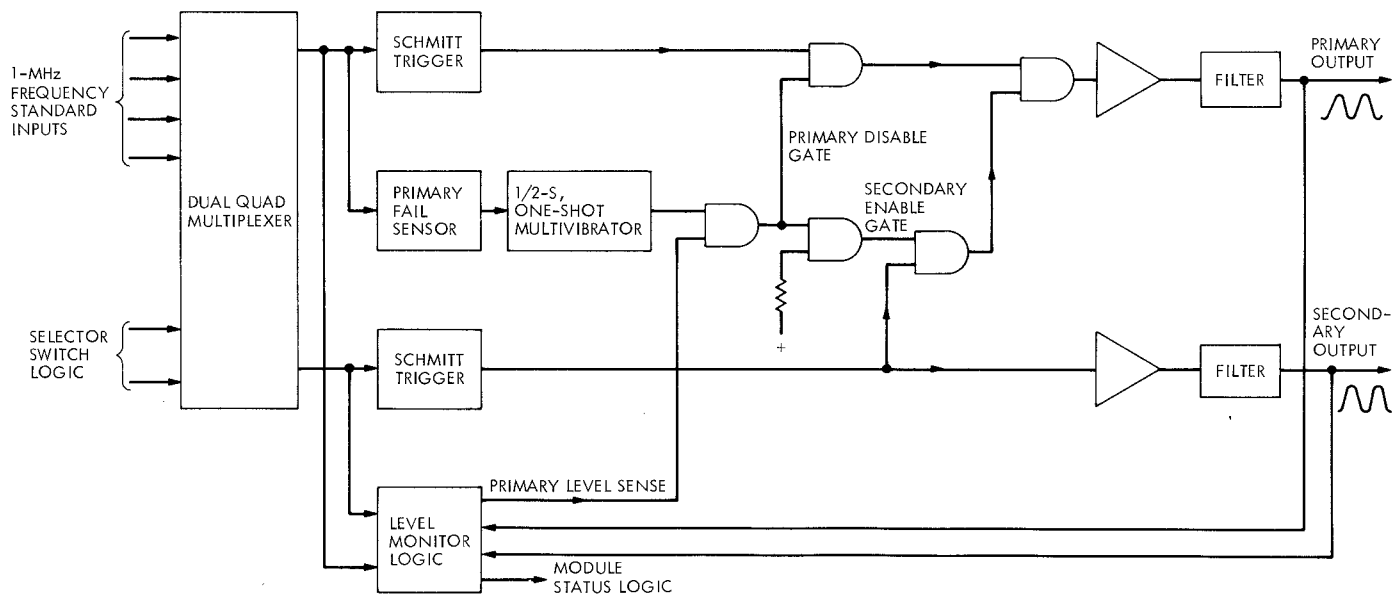


Fig. 2. Functional block diagram, 1-MHz clock reference switch